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Fault Tolerant Parallel DA Based Reconfigurable FIR Filters

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Abstract**:** *In signal processing, filters are used to remove unwanted portions of the signal, such as random noise, or to extract useful parts of the signal, such as the components lying within a specific frequency range. A reconfigurable FIR filter is a filter whose filter coefficients dynamically change during execution time. Such type of filters play an important role in many electronic circuits like digital up- down converters, software defined radio systems and multiple channel filters. Such systems should be highly reliable. This paper aims at developing a system that would be able to detect and correct the errors in the filter output automatically. This will be realized by making use of simple error correction codes.*

Keywords-*Finite Impulse Response (FIR) Filter, Distributed Arithmetic (DA) Algorithm, Reconfigurability Error Correction Codes, Hamming Codes, Fault Tolerance.*

1. Introduction

A finite impulse response (FIR) filter is a filter structure that can be used to implement practically any kind of frequency response in a digital manner. The implementation of FIR filters was initially consisted of a multiplication block, adder block, and flip-flops. The flip flops acted as registers to store the data temporarily. This approach was then replaced by another technique known as the multiple-constant-multiplication (MCM). But, this method is not suitable in cases where the filter coefficients dynamically change during runtime. While using the general multiplier-based structure, it requires a large chip area and consequently compels some limitations on the maximum possible filter order that can be realized for high-throughput applications.

In order to meet the requirements of high performance and reduce complexity, various algorithms were developed in course of time. Among these, a distributed arithmetic (DA)-based technique has gained substantial popularity in recent years for its high-throughput processing capability and increased regularity. Distributed Arithmetic is a computation algorithm that performs multiplication using pre-computed lookup tables (LUTs) instead of logic. DA is very much suitable to be implemented on homogeneous field-programmable gate arrays (FPGAs) since it can provide high utilization of available LUTs. For the modern heterogeneous FPGAs that contain built-in multiplier circuits, it has many advantages because it provides area savings for implementing digital filters. DA targets the sum-of-products (or vector dot product) operation, and many digital signal processing (DSP) tasks such as filter implementation, matrix multiplication and frequency transformation can be reduced to one or more sum-of-products computations. However, it is increasingly common to find systems in which several filters operate in parallel, in which the filters process different inputs with the same impulse response. Many techniques have been proposed for implementing fault tolerance in such systems which include Triple Modular Redundancy. It was shown in some previous works that with only one redundant copy, single error correction can be implemented. Here, we make use of simple Hamming codes for detecting the errors and then for correcting them. This scheme can also be used to provide more powerful protection using advanced error correction codes that can correct failures in multiple modules.

2. Reconfigurable FIR Filters

Reconfigurable FIR filters are those digital signal processing circuits in which filter order or coefficients can be dynamically changed depending inputs [3], [4]. In other words, the multiplication operation can be cancelled when the data sample to be multiplied to the coefficient is very small as to reduce the effect of partial sum in FIR filter. In the case of direct form of FIR filters, the multiplier coefficients are actually the coefficients in the transfer function. For an FIR filter, the direct form realization can be straight obtained from the convolution sum. The direct form circuit of an FIR filter is shown below.

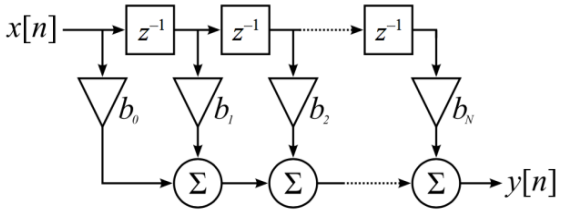

Figure. 1. Direct form of an FIR filter

This form is practical for filters used for small applications, but is inefficient and impractical for complex system designs 1since they become numerically unstable. An ordinary multiplier-based structure requires a large chip area for implementation and hence, it imposes limitations on the maximum possible filter order that can be realized for high-throughput and complex applications. The conventional multiplier based structure is not suitable in cases where the filter coefficients have to be varied dynamically, since the operation itself is multiple constant multiplications. Hence, as an alternative, another technique called Distributed Arithmetic is made use for implementing reconfigurable FIR filter.

3. Architecture for Reconfigurable Fir Filter

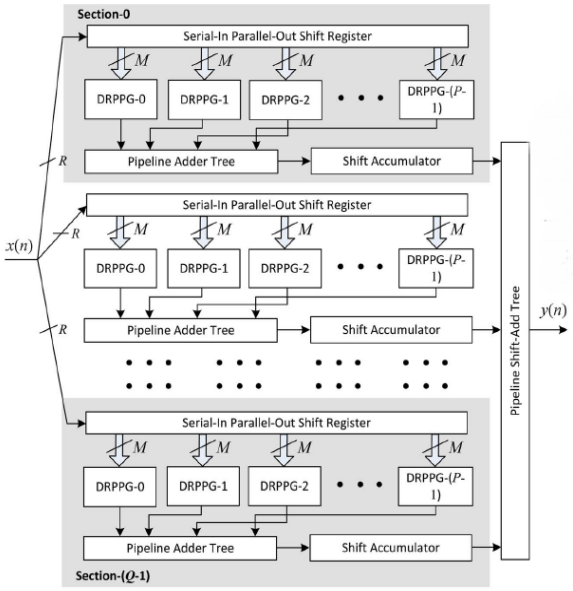

Figure. 2 .Structure of reconfigurable FIR filter in FPGA

Field-programmable gate arrays (FPGAs) have substantial resources of logic gates and random access memory blocks that can implement many complex digital computations.But, registers are inadequate resource in FPGA since many FPGA devices contain only two bits of registers. Therefore, in this architecture, the LUTs are being realized using Distributed RAM to overcome this constraint and are called RAM based LUTs [5].

The structure consists of serial in parallel out (SIPO) shift registers, distributed RAM based partial product generators (DRPPG), pipeline adder trees, shift accumulator and pipeline shift add tree. The whole system is divided into Q sections. In each section, P number of DRPPGs and PATs carry out the rightmost summation. The shift accumulator operates for R number of cycles depending on the second summation. The total size of the LUT is reduced two times since the DRPPGs from two different sections are sharing a single DRAM. The structure of DRPPG with shared DRAM is shown below [1].

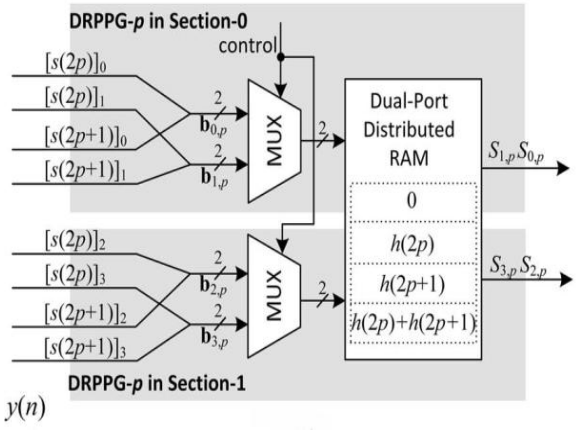

Figure. 3. Structure of DRPPG with shared DRAM

The partial inner products generated by the above structure are added together by the PAT. Over R clock cycles, these outputs are accumulated by the shift accumulator. The PSAT then produces the filter output every *R* cycles by using the output from each section. The accumulated value is reset every *R* cycles by the acc_rst control signal to make the accumulator register ready for being used in calculating the next output.

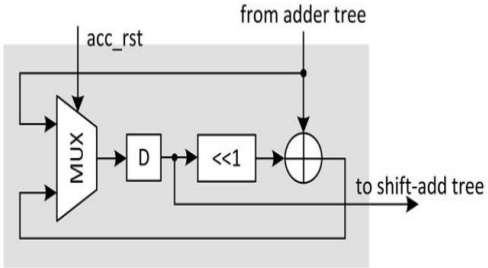

Figure. 4 .Structure of shift accumulator

4. Error Correction Codes

Error correction codes (ECC) allow data that is being read or transmitted to be checked for errors and, if necessary, corrected on the fly. It differs from parity checking in the way that along with detection, errors are also corrected. They are mainly designed for storing data and transmission

hardware as data rates. Error-correcting codes find use in cellular phones, CD players and high speed modems.

A simple ECC takes a block of *k* bits to produce a block of *n* bits on adding *n*−*k* parity check bits [6]. By properly designing some XOR combinations of data bits as the parity check bits, it is possible to detect and correct errors.

Hamming codes are a class of linear error-correction codes that are able to detect up to two bit errors and correct one bit errors. A simple parity code can detect only an odd number of error bits cannot correct errors. Hamming codes are also called perfect codes, due to the fact that they achieve the highest rate of code with their block length and minimum distance of three.

Consider a simple (7, 4) hamming code [7]. The parity check bits for the corresponding code, in terms of data bits *x1, x2, x3* and *x4* can be obtained as follows.

$$p1 = x1 \oplus x2 \oplus x3$$
$$p2 = x1 \oplus x2 \oplus x4$$
$$p3 = x1 \oplus x3 \oplus x4$$

The data and parity check bits are stored and can be recovered later. This can be done by recomputing the parity check bits. The results are compared with the already stored values. In the example taken, an error on data *x1*will cause errors on all the three parity check bits *p1*, *p2* and *p3*; Similarly, an error on *x2* causes error in *p1* and *p2*; an error on *x3* causes error in *p1* and *p3*, and finally an error on *x4*causes error in *p2* and *p3*. Thus the error data bit can be identified and can be corrected.

The overall architecture for implementing fault tolerance in parallel FIR filters is shown below.

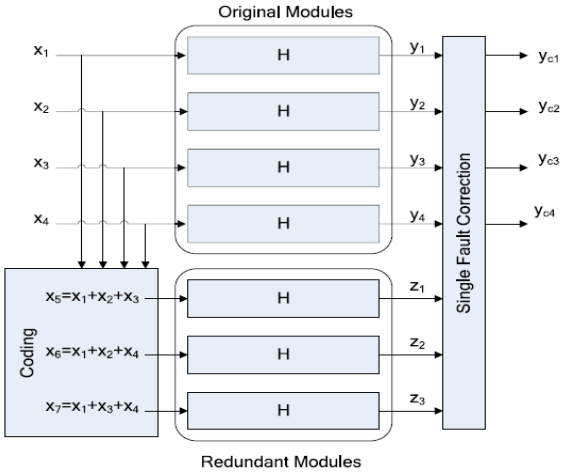

Figure. 5. Error correction scheme block diagram

This scheme can be applied to a set of parallel filters by defining a set of check filters *zi*. The checking is done by testing whether:

$$z1[n] = y1[n] + y2[n] + y3[n]$$
$$z2[n] = y1[n] + y2[n] + y4[n]$$
$$z3[n] = y1[n] + y3[n] + y4[n].$$

Any error on filter *y*1 will cause errors on the check filters *z*1, *z*2, and *z*3. In the same way, errors on the other filters will cause errors on another set of *zi* [2].

Once the error is detected, correction is achieved by reconstructing the error prone outputs using the rest of the data and check filter outputs. i.e., when an error is detected on $y1$, it can be corrected by the following equation:

$$yc1[n] = z1[n] - y2[n] - y3[n]$$

Similar equations can be derived and used to correct errors on the other data outputs.

5. Conclusion

In this brief, a system of parallel reconfigurable FIR filters with error detection and correction capability is discussed. These types of systems are common in multichannel communication systems, Distributed arithmetic algorithm is used for realizing the filter and hamming codes are used for implementing fault tolerance. The technique can be used for protecting parallel filters that have the same impulse response and process input signals of different values.

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